What is claimed is:

1. A semiconductor device, comprising:

a semiconductor substrate;

a first metal layer formed overlying the semiconductor substrate;

an etch stop layer formed overlying the first metal layer and the semiconductor substrate;

a dielectric layer formed overlying the etch stop layer; and

a second metal layer penetrating the dielectric layer and the etch stop layer and electrically connected to the first metal layer;

wherein, the etch stop layer has a dielectric constant smaller than 3.5; and

wherein, the dielectric layer has a dielectric constant smaller than 3.0.

2. The semiconductor device of claim 1, wherein the etch stop layer has a compressive stress of $0\sim1\times10^{9}$ dynes/cm^{2}.

3. The semiconductor device of claim 2, wherein the dielectric layer has a tensile stress approximating to the compressive stress of the etch stop layer.

4. The semiconductor device of claim 1, wherein the dielectric layer has a film hardness greater than 0.2GPa and an elastic modulus greater than 5GPa.

5. The semiconductor device of claim 1, wherein the etch stop layer is an oxygen-doped silicon carbide (SiOC) layer, and the dielectric layer is a porous organo-silicate glass (OSG) layer.

6. The semiconductor device of claim 1, wherein each of the first metal layer and the second metal layer is a copper layer.

7. The semiconductor device of claim 1, wherein the etch stop layer is a composite film comprising a first etch stop layer and a second etch stop layer, in which the first etch stop layer is formed overlying the second etch stop layer.

8. The semiconductor device of claim 7, wherein a first etching selectivity S_1 of the first etch stop layer to the dielectric layer, and a second etching selectivity S_2 of the second etch stop layer to the dielectric layer satisfy the formula: $S_1 \neq S_2$.

9. The semiconductor device of claim 8, wherein S_1 and S_2 satisfy the formula: $0<S_1<S_2$.

10. The semiconductor device of claim 7, wherein a first thickness T_1 of the first etch stop layer and a second thickness T_2 of the second etch stop layer satisfy the formula: $T_2 < (T_1+ T_2)/3$.

11. The semiconductor device of claim 7, wherein the etch stop layer is a SiCO-based composite deposition.

12. The semiconductor device of claim 11, wherein the first etch stop layer is a SiC film and the second etch stop layer is a SiO film.

13. The semiconductor device of claim 7, wherein each of the first etch stop layer and the second etch stop layer

is SiCN, SiCO, SiN, SiON, SiC, or SiO, or a combination thereof.

14. A copper damascene structure, comprising:

a semiconductor substrate;

a first copper layer formed overlying the semiconductor substrate;

an etch stop layer formed overlying the first copper layer and the semiconductor substrate;

a dielectric layer formed overlying the etch stop layer, in which a damascene opening is formed to penetrate the dielectric layer and the etch stop layer to expose the first copper layer; and

a second copper layer formed in the damascene opening and electrically connected to the first copper layer;

wherein, the etch stop layer has a dielectric constant smaller than 3.5; and

wherein, the dielectric layer has a dielectric constant smaller than 3.0.

15. The copper damascene structure of claim 14, wherein the etch stop layer has a dielectric constant of 1.0~3.5, and the dielectric layer has a dielectric constant of 1.0~3.0.

16. The copper damascene structure of claim 14, wherein the etch stop layer has a compressive stress of $0\sim1\times10^9$ dynes/cm^2.

17. The copper damascene structure of claim 16, wherein the dielectric layer has a tensile stress approximating to the compressive stress of the etch stop layer.

18. The copper damascene structure of claim 14, wherein the dielectric layer has a film hardness greater than 0.2GPa and an elastic modulus greater than 5GPa.

19. The copper damascene structure of claim 14, wherein the etch stop layer is an oxygen-doped silicon carbide (SiOC) layer, and the dielectric layer is a porous organo-silicate glass (OSG) layer.

20. The copper damascene structure of claim 14, wherein the second copper layer is a copper single damascene structure or a copper dual damascene structure.

21. The copper damascene structure of claim 14, wherein the etch stop layer is a composite film comprising a first etch stop layer and a second etch stop layer, in which the first etch stop layer is formed overlying the second etch stop layer.

22. The copper damascene structure of claim 21, wherein a first etching selectivity S_1 of the first etch stop layer to the dielectric layer, and a second etching selectivity S_2 of the second etch stop layer to the dielectric layer, satisfy the formula: $S_1 \neq S_2$.

23. The copper damascene structure of claim 22, wherein at least one of S_1 and S_2 is larger than zero.

24. The copper damascene structure of claim 22, wherein S_1 and S_2 satisfy the formula: $0<S_1<S_2$.

25. The copper damascene structure of claim 21, wherein a first thickness T_1 of the first etch stop layer and a second thickness T_2 of the second etch stop layer satisfy the formula: $T_2 < (T_1 + T_2)/3$.

26. The copper damascene structure of claim 21, wherein the etch stop layer is a SiCO-based composite deposition.

27. The copper damascene structure of claim 26, wherein the first etch stop layer is a SiC film, and the second etch stop layer is a SiO film.

28. The copper damascene structure of claim 21, wherein each of the first etch stop layer and the second etch stop layer is SiCN, SiCO, SiN, SiON, SiC, or SiO, or a combination thereof.

29. A fabrication method for a semiconductor device, comprising the steps of:

providing a semiconductor substrate having a first metal layer;

forming an etch stop layer overlying the first metal layer and the semiconductor substrate, wherein the etch stop layer has a dielectric constant smaller than 3.5;

forming a dielectric layer overlying the etch stop layer, wherein the dielectric layer has a dielectric constant smaller than 3.0;

forming an opening which penetrates the dielectric layer and the etch stop layer and exposes the first metal layer; and

forming a second metal layer in the opening, in which the second metal layer is electrically connected to the first metal layer.

30. The fabrication method for a semiconductor device of claim 29, wherein the etch stop layer has a compressive stress of $0\sim1\times10^9$ dynes/cm^2, and the dielectric layer has a tensile stress approximating to the compressive stress of the etch stop layer.

31. The fabrication method for a semiconductor device of claim 29, wherein the dielectric layer has a film hardness greater than 0.2GPa and an elastic modulus greater than 5GPa.

32. The fabrication method for a semiconductor device of claim 29, wherein the etch stop layer is an oxygen-doped silicon carbide (SiOC) layer, and the dielectric layer is a porous organo-silicate glass (OSG) layer.

33. The fabrication method for a semiconductor device of claim 29, wherein the opening filled with the second metal layer is a copper damascene structure.

34. The fabrication method for a semiconductor device of claim 29, wherein the etch stop layer is a composite film comprising a first etch stop layer and a second etch stop layer, in which the first etch stop layer is formed overlying the second etch stop layer.

35. The fabrication method for a semiconductor device of claim 34, wherein a first etching selectivity S_1 of the

first etch stop layer to the dielectric layer, and a second etching selectivity S_2 of the second etch stop layer to the dielectric layer satisfy the formula: $S_1 \neq S_2$.

36. The fabrication method for a semiconductor device of claim 35, wherein S_1 and S_2 satisfy the formula: $0<S_1<S_2$.

37. The fabrication method for a semiconductor device of claim 34, wherein a first thickness T_1 of the first etch stop layer and a second thickness T_2 of the second etch stop layer satisfy the formula: $T_2 < (T_1 + T_2)/3$.

38. The fabrication method for a semiconductor device of claim 34, wherein the etch stop layer is a SiCO-based composite deposition.

39. The fabrication method for a semiconductor device of claim 38, wherein the first etch stop layer is a SiC film, and the second etch stop layer is a SiO film.

40. The fabrication method for a semiconductor device of claim 34, wherein each of the first etch stop layer and

the second etch stop layer is SiCN, SiCO, SiN, SiON, SiC, or SiO, or a combination thereof.